LOW POWER DATA STORAGE ELEMENT WITH ENHANCED NOISE MARGIN

ABSTRACT OF THE DISCLOSURE

A data storage element for use in LSSD compliant circuit designs. The data storage element has an alternate, or scan, data input circuit that has increased immunity to electrical noise while maintaining lower power consumption than the circuits used for primary data input. This increased noise immunity reduces the probably that noise on the alternate data input will cause an unintended change of data state stored in the data storage element. Modification of latch circuits used in the data storage element allow a reduction in the number of transistors used in the latch circuits, thereby compensating for the increase in transistors used in the alternate data input circuit and allowing the data storage element to use the same number of transistors as prior designs that have less noise immunity on their alternate data inputs.